DC Biased Input Stage with Differential Photocurrent Sensing for VLC Front-Ends

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***Abstract*—The reverse bias voltage across the PIN photodiode is essential for the photodiode to operate in the photoconductive mode. This paper presents an input bias stage with differential photocurrent sensing for VLC front-ends. The bias voltage is provided from within the transimpedance amplifier's (TIA) circuit eliminating the need of external bias voltage. The amount of bias voltage could be optimised according to the photodiode required sensitivity and capacitance. The differential configuration makes the TIA immune to any common mode noise. The proposed method is applied to a hypothetical TIA and results are compared with single ended structure. Simulation results showed that using this approach it is possible to achieve a transimpedance gain of 120 dBΩ over a maximum bandwidth of 14.5 MHz with a common mode rejection ratio of 61 dB while the circuit provides a controlled bias voltage of up to 6 V across the PIN photodiode eliminating the need for external bias voltage source.**

Keywords-Positive-Intrinsic-Negative (PIN); transimpedance amplifier (TIA); visible light communications (VLC)

I. INTRODUCTION

Recently, visible light communication systems (VLC) have attracted researchers' attention as a reliable solution to the rapid demand of high speed wireless communications. The idea of VLC systems is based on the dual use of LEDs for both illumination and data communications. LEDs are considered ideal light sources due to a number of features: high illuminance, low power consumption, and long-life span. In addition, LEDs have high switching capability as they can be switched between ON and OFF states at high speeds enabling them to be used in high data rates communications [1]. A recent study successfully demonstrated high efficiency indoor VLC system capable of providing standard room illumination as well as a wide coverage optic wireless communication over a distance of 2.3m using commercial white light phosphor LEDs [2].

VLC depends mainly on line of sight configuration which require sensitive photodiodes. The required photodiode sensitivity can be achieved by two main methods, having high gain amplifiers, increasing the photodiode area or using a combination of both methods. The most common problem using these methods is bandwidth limitation due to the high capacitance of large area photodiodes [3].

PIN photodiodes have been widely used in optical wireless communications due to the following feature: 1) their high sensitivity to visible light operating wavelength; 2) high response speed; 3) their low noise because of the thickness of intrinsic region which could be optimised to the required transient response and frequency response [4]. Fig. 1 shows the PIN equivalent circuit. The photocurrent generated by the photodiode could be represented by a current source Ip. The photodiode's parasitic capacitance and shunt resistance can be represented by the capacitor and resistor Rsh and Cp. The series resistance Rs takes in account both resistance in homogenous region of diode and contact parasitic resistance. During the PIN photodiode operation, a reverse bias voltage is applied to ensure that the intrinsic region is depleted from any charges. If the photodiode operates without reverse bias, the photocurrent will be distributed between the shunt resistance and the load resistance creating a forward bias voltage reducing its ability to be a constant current source.

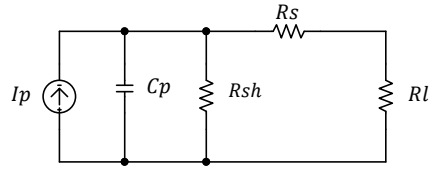

Figure 1. PIN photodiode equivalent circuit

In most VLC front-ends the photodiode current sensing is single-ended which means that only the photocurrent produced from the anode is used while the cathode current is not effectively used. This will cause in halving the current signal and asymmetry in the differential structure which requires adding a shielded dummy photodiode to re-balance the circuit as in [5], [6]. Fig. 2 shows the conventional single-ended TIA model. In [7], [8] differential photodiode current sensing structures based on regulated cascode input stage were deigned. Both designs provide a fixed bias voltage across the photodiode. Another structure in which cross–coupled CMOS pair added to a differential common gate input stage current amplifier was discussed and implemented in [9]. This study proposes an input bias stage design with differential photodiode current sensing. The required reverse bias voltage across the PIN photodiode is obtained by two DC level shift input stages biased with two opposite current mirrors. The amount of reverse bias voltage across the PIN photodiode could be controlled by the DC level shift resistances according to the required sensitivity. The proposed design is simulated using BJT devices as they are superior to MOSFET devices in voltage gain, low noise characteristics and high sensitivity to low input currents applications.

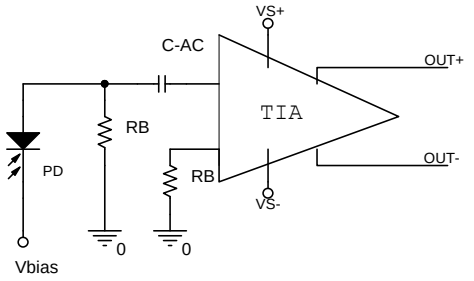

Figure 2- Single-ended conventional TIA model

This paper is organized in five sections. Section II depicts a short overview on the proposed input bias stage. Section III presents circuit design and consideration. Section IV presents the simulation results for proposed design compared to single ended structure. Finally, section V presents the conclusions and discussion.

II. PROPOSED PHOTODIODE BIAS STAGE

Fig. 3 depicts the proposed bias stage applied to a hypothetical TIA.

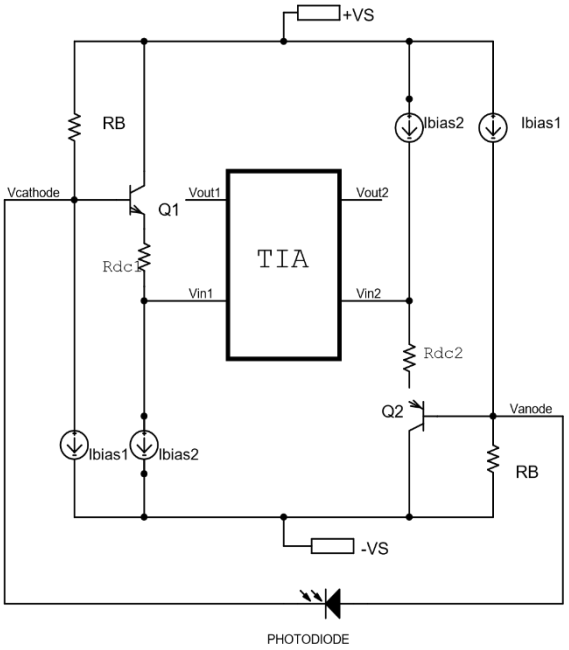

Figure 3. Proposed bias circuit applied to a hypothetical TIA

The proposed structure is comprised of two opposite DC level shift input stages. The DC level shift is in fact a CC configuration where the signal is applied to the base and output is taken from the emitter [10]. From the large signal stand point the output voltage of each stage is given by:

$$V_{cathode} = V_{in1} - V_{be}\,Q1 - V_{Rdc1} \quad (1)$$

$$V_{anode} = -V_{be}\,Q2 - V_{Rdc2} - V_{in2} \quad (2)$$

In the above equations: V_{be} is the base emitter voltage of the input stage transistor and V_{Rdc} is the voltage drop across the DC level shift resistance Rdc. The NPN transistor Q1 with the resistor $Rdc1$ provides a positive DC shift while the PNP transistor Q2 with the resistor $Rdc2$ provides a negative DC shift. The biasing current sources are present to establish the quiescent DC operating current in the emitter-follower transistors Q1 and Q2. The reverse bias on the photodiode is determined by the total DC shift obtained at both Cathode and Anode, which could be controlled by the values of $Rdc1$ and $Rdc2$ and the bias currents. The resistance RB with the bias current $Ibias1$ controls the DC offset level at the terminals of the photodiode.

III. CIRCUIT DESIGN AND CONSIDERATION

Fig. 4 depicts the simplified schematic of the proposed fully differential TIA. It is assumed that the input photocurrent is driven by a current source, with an intrinsic capacitance Cp and a shunt resistance Rsh representing the photodiode. The differential amplifier comprises two identical transistors Q3 and Q4 coupled in a symmetric manner at their emitters with a DC bias current provided by a current source. The output currents are available at the collectors of Q3 and Q4. Conversion to output voltage is achieved by incorporating equal collector loads RC connected to the positive voltage supply VS. the bias currents $Ibias1$, $Ibias2$ and the tail current are supplied by two beta helper current mirrors.

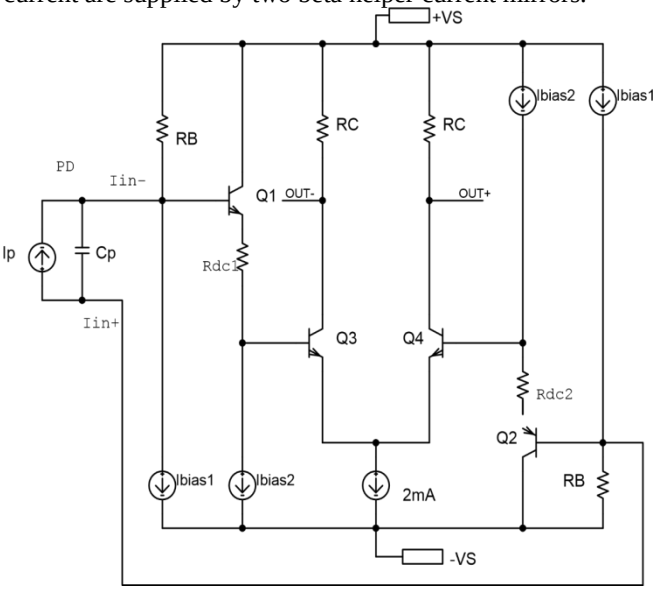

Figure 4. Schematic diagram of the Proposed fully differential TIA

A. Circuit Analysis

To evaluate the limitations of the proposed method it is necessary to apply AC small signal analysis. By looking at the differential mode half circuit for simplification, the design is comprised of a CC input bias stage cascaded with a common-emitter (CE) stage. The amplifier transimpedance gain and voltage gain can be expressed as:

$$A_{TIA} \approx \frac{\beta^2 Rc}{1+\beta(r_{e1}+r_{be2}+Rdc)/RB} \quad (3)$$

$$A_v \approx \frac{\beta Rc}{r_{e1}+r_{be2}+Rdc} \quad (4)$$

In the above equations: r_{e1} is the resistance seen at the emitter of Q1 and Q2, r_{be2} is the base-emitter resistance seen at the base of Q3 and Q4, and β is the dc current gain. The current gain of the composite design is obtained from the two stages CC and CE which offers an additional gain advantage to the proposed bias stage. In this design, the amplifier voltage gain is obtained from the CE stage which suffers from the Miller effect feedback capacitance which limits the amplifier bandwidth.

B. *Differential Design Advantages over Single Ended Structures*

The proposed design is fully differential which has the following advantages over the single ended structures: first the differential sensing of the photodiode means the signal is detected from both the anode and the cathode, therefore using the whole input signal effectively rather than being detected from the anode as in single ended structure. Secondly, fully differential structure avoids asymmetry in single-ended designs. Since the photodiode is placed across the differential inputs of the TIA, the resulting circuit is balanced eliminating the need of a dummy matching capacitor as well as rejecting the common mode noise caused by the DC bias voltage. Finally, the ability to control the amount of reverse bias voltage across the photodiode is useful to optimize the required photodiode capacitance.

IV. Simulation Results and Discussion

Simulation were run to compare the differential structure, which uses the DC level shift input stage topology of Fig. 3 with single ended conventional structures of Fig. 2. All simulations were carried out using OrCAD 16.6 software tool.

TABLE I. Components Values Used and Bias Currents

Component	Type	Value	Bias current mA
Q2	PNP-BFT92	$\beta = 45$	—
Q1 Q3-Q4 Q5-Q6 Q7-Q8	NPN-BFT25A	$\beta = 60$	—
RB	—	8KΩ	0.2
RC	—	3.5KΩ	1
$Rdc1$	—	100Ω	5.35
$Rdc2$	—	100Ω	7.5
Rsh	—	100MΩ	—
Cp	—	4pF	—

The same transistors types, resistors and bias currents were used in all cases. As there is no small signal mode for PIN photodiodes, the photodiode electrical parameters were modeled using data for (OSD15-5T) photodiode. A parasitic capacitor of 4pF and a shunt resistor of 100MΩ were chosen for the PIN photodiode equivalent circuit. The photodiode current source was simulated using an IPWL programmable current source. An optic signal with an amplitude of 2µA and 10ns, 10ns, 400ns rise time fall time and duration respectively were used. For the single-ended structures the input signal is driven through an RC coupling circuit. A capacitor of 0.01µF was chosen. A dual supply voltage of +5V, -5V and the same value of bias resistance RB were used in both designs. Table I shows transistors types, resistors and bias currents used in simulations.

A. *Simulation Results*

Fig. 5 shows the pulse response of proposed and single-ended structures. The first wave represents the photocurrent signal generated by the photodiode. The second wave represents the output voltage of the single-ended structure and the third wave represents the output voltage of the proposed fully differential design. Simulation results showed that the proposed design could achieve a maximum transimpedance gain of 1.029MΩ, which clearly appears in the voltage swing of the pulse response from -1V to 3V, while the single-ended design's maximum transimpedance gain was 150KΩ. The gain using the proposed method was more than twice of the single-ended structure because of the additional current gain achieved by the CC stage. The slew rate for the output signals were $30V/\mu s$ and $5V/\mu s$ for the differential and single-ended waves respectively. The frequency response of the differential and single-ended structures is shown in Fig. 6. The dashed line represents the single-ended bandwidth while the solid line represents the proposed differential bandwidth curve. The bandwidths of the differential and single-ended structures were 14.5MHz and 4.82MHz respectively. Results showed a bandwidth improvement by using the proposed design.

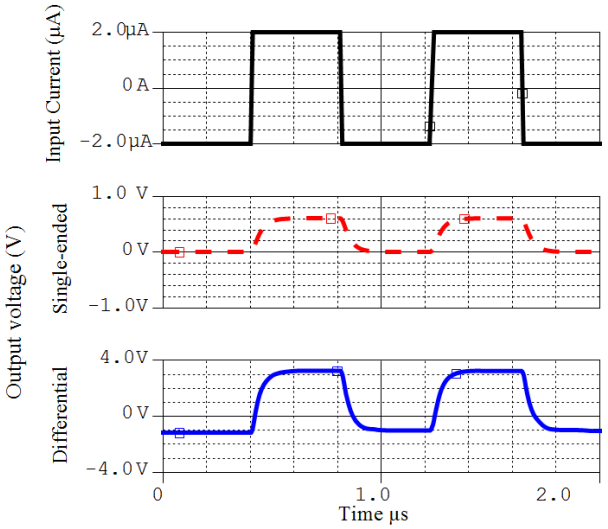

Figure 5. Pulse response of single-ended and proposed fully differential structures

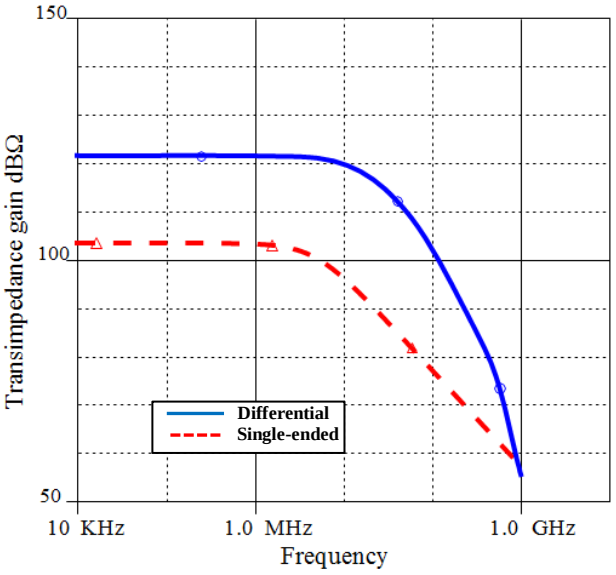

Figure 6. Frequency response of single-ended and proposed fully differential structures

V. Conclusions and Discussion

An input bias stage suitable for VLC front-ends has been presented. The proposed structure is based on using the CC level shift configuration as an input stage to provide the required bias voltage across the photodiode. Simulation have shown that by using the proposed structure a transimpedance gain of an order of magnitude higher than single-ended structures can be achieved as was predicted by equation (4). In addition, results showed a bandwidth improvement by using this approach. The design could provide a reverse bias voltage of up to 6V however, this trades-off lower gain and bandwidth due to interaction of the value of the DC shift resistance. The transimpedance gain of the design is dependent on the value of the bias resistance RB which was set to an optimum value of 8kΩ for the highest achievable gain. The proposed design speed determined by the amplifier slew rates showed improvement over single-ended structure. To overcome the high input impedance of the CC input stage and improve the front-end performance low capacitance PINs (expensive) can be used. Future work should be directed towards incorporating the proposed input bias stage in low input impedance configurations to isolate the photodiode's high capacitance. Higher gains could be achieved by using differential amplifiers with active loads instead of resistor loads.

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