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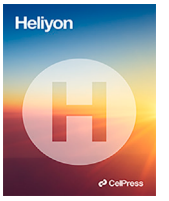

Research article

An event-triggered synchronization strategy for high-precise clock systems with switching topologies

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ABSTRACT

The clock synchronization is a key technology for the reliability of wireless sensor networks (WSN). To reduce the communication burden and address the challenge of clock synchronization for high-precise clock systems in WSN with switching topologies, this paper proposes an event-triggered synchronization strategy for high-precise clock systems. Firstly, based on the concept of offset and skew, the model of whole clock systems is investigated and an event-triggered strategy is proposed for high-precise clock systems with switching topologies. Then, a synchronization strategy for clock systems is presented to achieve clock synchronization with the convergence of clock offset and clock skew. The sufficient condition for the synchronization of high-precise clock systems with switching topologies is obtained. Afterwards, the optimal event-triggered weighting matrices and controller gains are calculated by converting the clock synchronization problem as a solvable optimization problem. Finally, the performance of the proposed clock synchronization method is evaluated by simulations.

1. Introduction

With the development of science and technology, the Internet of Things (IoT) have been closely related to human life. Specially, the Industrial Internet of Things (IIoT) have become the common research hotspot in academia and industry fields. As a key technology in IIoT, the industrial wireless sensor networks (WSN) can solve the perception, communication, and control problems of moving plants in industrial environments or plants that cannot be wired in harsh environments [1–4]. Because industrial systems have strict requirements for real-time and deterministic performance, it is critical to ensure that the devices connected to WSN have high-precise clocks for data acquisition and system control. The clock synchronization means that the sensor and actuator nodes in a network have the same time base and the clocks in WSN should be synchronized. The clock synchronization technology is an important supporting technology of WSN. Many applications of WSN need clock synchronization as the premise. The industrial wireless technology is the continuation of WSN technology. In general, the industrial WSN have higher requirements for real-time and reliability. The high-precise clock synchronization mechanism will play a decisive role in the real-time performance of industrial WSN.

In recent years, the clock synchronization technology has begun to develop rapidly. Scholars from all over the world are actively committed to the research of clock synchronization and have proposed a variety of clock synchronization protocols [5–8]. From the perspectives of network communication and clock synchronization packet exchange, the clock synchronization can be divided into

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synchronization protocols based on receiver-receiver and sender-receiver [9,10]. In the control field, the clock synchronization can be regarded as a consensus problem, and then the appropriate controller is designed for clock synchronization. For example, Jia et al. investigated a disturbance compensation strategy for clock synchronization based on proportional-integral observer [11]. Then with the proposed a zero-pole optimal algorithm, the clock synchronization for a network can be achieved. In reference [12], Wu et al. adopted a layered and distributed control structure to design the global phase and frequency synchronization control scheme for the Kuramoto type oscillator network with random interference in the communication channel.

Due to the high precision of clock synchronization algorithm, the higher requirements are put forward for the reliability of WSN. However, for the high value of clock information in transmission network, it is often subjected to various strong interference and even network attacks. The switching of communication topology is one of the common consequences of strong interference and network attacks. In fact, the switching topologies are often occurred because of fast information exchange and channel fading [13]. The consensus problem of the network with switching topologies has attracted widely attention [14–18]. For high-precise clock systems, the switching topologies have an important impact on the accuracy of clock synchronization, and even affect whether the clock systems can achieve clock synchronization. Therefore, it is necessary to study clock synchronization under switching topologies, especially when the interference is subjected in WSN. But there exists little research concerned about the clock synchronization problem with switching topologies, which is the first motivation of this paper.

For high-precise clock systems, the transmission of clock information is usually characterized by high frequency. How to save communication resource for realizing the effective use of WSN is one of the problems that needs to be concerned. The event-triggered strategy is a control mode based on preset triggered condition. If a control task meets the triggered condition, an event occurs. In this case, the system executes the triggered task to transfer information between neighbors or update the controller [19–21]. It can effectively reduce the execution times of control tasks and solve the problem of high frequency communication [22]. In the consensus control for intelligent systems, the control algorithm based on event-triggered mechanism has achieved a lot of results, such as control for autonomous vehicles, high-speed trains, robot systems, and satellite systems, et al. For example, by utilizing CARLA simulator, Zhou et al. [23] proposed an event-triggered scheme for vehicle path tracking with fewer control sequences. In reference [24], a distributed event-based cooperation scheme was investigated for railway trains. Li et al. [25] studied an event-triggered command mechanism for robot manipulators to eliminate the communication burden. Zhao et al. [26] presented a hybrid event-based method for the application of satellite formation problem. However, in the field of clock synchronization, only Jia et al. [27] proposed an event-triggered synchronization scheme for clock systems. The event-triggered synchronization scheme for clock systems still needs to be further studied. To reduce the communication burden of high-precise clock systems, it is imperative to investigate the clock synchronization control with event-triggered scheme, which is the second motivation.

In general, for the clock systems in industrial WSN, the clock accuracy needs to be sub-microsecond or even microsecond. Hence, it is essential to design an accurate clock synchronization mechanism for high-precise clock systems. In this paper, we attempt to develop an event-triggered synchronization strategy for high-precise clock systems with switching topologies. The contributions of this paper are given as follows:

1. A clock model of the clock node is established. With the concept of offset and skew, the model of whole clock systems is illustrated with switching topologies. Besides, an event-triggered strategy is proposed for high-precise clock systems.
2. A synchronization strategy for clock systems with switching network topologies is presented and the sufficient condition for the synchronization of high-precise clock systems with switching topologies is obtained.
3. The clock synchronization problem for clock systems is described as an optimization problem. By solving the optimization problem, the optimal event-triggered weighting matrices and controller gains can be obtained.

2. Problem formulation

In this section, the model of clock systems which consists N unperfected clock nodes and a reference clock node in WSN is first given. Then the communication framework of clock systems with switching topologies and the event-triggered scheme are presented.

2.1. Clock model

In WSN, the local clock information is usually given by a crystal oscillator which is operating with a specific frequency. The reference clock is an ideal clock which the frequency deviation of crystal oscillator is always zero. In fact, the crystal frequency of clock is often affected by the crystal itself and the external environment, which means the clock is a biased clock and has the frequency deviation and phase noise.

For the unperfected clock i, set $c_i(k)$ and $\gamma_i(k)$ as the clock value and clock rate, respectively. For a free clock, the clock value of clock node i can be represented as

$$c_i(k+1) = c_i(k) + \gamma_i(k)h + \omega_{ci}(k) \tag{1}$$

where h is the sample interval and $\omega_{ci}(k)$ is the phase noise.

Generally, the clock rate often exists a certain amount of randomness due to the changes of temperature, power supply, and mechanical vibration, etc. The dynamic of clock rate can be described as

$$\gamma_i(k+1) = \gamma_i(k) + \omega_{\gamma i}(k) \tag{2}$$

where $\omega_{\gamma i}(k)$ is the clock rate noise which is depended on the disturbance $f_i(k)$ and noise $\varepsilon_i(k)$. Therefore,

$$\omega_{\gamma i}(k) = f_i(k) + \varepsilon_i(k). \tag{3}$$

Indeed, $f_i(k)$ is a periodic signal and $\varepsilon_i(k)$ can be described as a Gaussian process. Then define the clock state vector $x_i(k) = [c_i(k), \gamma_i(k)]^T$ and the clock disturbance signal $\omega_i(k) = [\omega_{ci}(k), \omega_{\gamma i}(k)]^T$. Hence, with (1) and (2), the state model of a free clock is given as

$$x_i(k+1) = Ax_i(k) + \omega_i(k) \tag{4}$$

where $A = \begin{bmatrix} 1 & h \\ 0 & 1 \end{bmatrix}$.

However, the equation (4) describes the free clock, which means the clock is updated according to its own deviation frequency and the deviation from the accurate reference clock is usually increasing. Therefore, to achieve the clock synchronization, it is necessary to design a controller to regulate the unperfected clock, so as to maintain the unperfected clock within a pre-defined synchronization error range and the clock synchronization of clock systems in WSN can be achieved.

Then, we add the control input to a clock node. The state space model of a clock with control input $u_i(k)$ is given as

$$x_i(k+1) = Ax_i(k) + Bu_i(k) + \omega_i(k) \tag{5}$$

where $B = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$.

In addition, the reference clock can be reformulated as

$$x_0(k+1) = Ax_0(k) \tag{6}$$

where $x_0(k) = [c_0(k), \gamma_0(k)]^T$. For the reference clock, we assume it is not affected by the phase noise and clock rate noise. In addition, the reference clock has a standard clock rate.

2.2. Communication framework of clock systems

In this subsection, we utilize the graph theory and Markov chain to describe the relationship among the clock nodes in WSN. First, we introduce the graph theory to describe the information relation of clock nodes in WSN.

The connection of N unperfected clock nodes is depicted by a graph $G(X, \varepsilon, \Lambda)$, where $X = \{x_1, x_2, ..., x_N\}$. $\varepsilon \subseteq X \times X$ is the communication edge set of unperfected clock nodes. $\Lambda = [a_{ij}]$ is the adjacency matrix which can describe the communication edges of clock nodes and $a_{ii} = 0$. (x_i, x_j) is the edge of clock node x_i to clock node x_j. If $(x_i, x_j) \in \varepsilon$, the clock node x_j is the neighboring clock node of x_i, $a_{ij} = 1$. If not, $a_{ij} = 0$. Set Δ as the diagonal in-degree matrix. The in-degree of clock node x_i is $\sum_{j=1}^{N} a_{ij}$, then the Laplace matrix of G is $L = \Delta - \Lambda$. In addition, $\tilde{G}$ presents the connection of N unperfected clock nodes and the reference clock node, and define $\Theta = diag\{\theta_1, \theta_2, ..., \theta_N\} \in R^{N \times N}$. If the reference clock node is a neighbor of clock node x_i, $\theta_i = 1$; otherwise, $\theta_i = 0$. If there exists a path in $\tilde{G}$ from every clock node x_i to reference clock node, then the reference clock node is globally reachable in $\tilde{G}$ [28,29]. We assume the reference clock node is globally reachable in this paper. For the time-varying communication topologies, the Markov chain is introduced to describe the topologies.

Define a switching signal χ_k $(k \in N^+)$ and $\chi_k \in S = \{1, 2, ..., q\}$ is a Markov chain. The communication graph of clock node systems keeps switching within $\tilde{G}(\chi_k) \in \{\tilde{G}(1), \tilde{G}(2), ..., \tilde{G}(q)\}$. $prob\{\chi_{k+1} = \eta | \chi_k = \beta\} = \pi_{\beta\eta}$ is the switching probability and $prob\{\chi_k = \beta\} = \pi_\beta(k)$. $\pi_{\beta\eta}$ is the single step transition probability from mode β to η and $\sum_{\eta=1}^{q} \pi_{\beta\eta} = 1$. $\pi_\beta(k)$ is the transition probability of $\tilde{G}(\beta)$ with initial probability $prob\{\chi_0 = \beta\} = \pi_{0\beta}$. Define $\Pi(k) = [\pi_1(k), \pi_2(k), ..., \pi_q(k)]^T$ to describe the probability distribution. Besides, $\Pi_0(k) = [\pi_{01}(k), \pi_{02}(k), ..., \pi_{0q}(k)]^T$ is the initial probability distribution. The transition probability matrix is $\pi = [\pi_{\beta\eta}]_{q*q}$ and $\Pi(k+1) = \pi^T \Pi(k)$ [30].

2.3. Event-triggered strategy and control objectives

Then we design the event-triggered scheme. For the unperfected clock node i, the state change of i-th clock node from the last event to time instant k is

$$e_i(k) = x_i(k) - x_i(k^i_{m_i}), \tag{7}$$

where $k^i_{m_i}$ is the m_i-th triggered instant for clock node i. The event-triggered condition for clock node i is

$$e_i^T(k)\Omega(\chi_k)e_i(k) \geq \delta_i(\chi_k)v_i^T(k)\Omega(\chi_k)v_i(k) \tag{8}$$

where $\Omega(\chi_k) > 0$ is the weighting matrix and $\delta_i(\chi_k)(i = 1, \cdots, N) > 0$ is the threshold parameter. In addition, $v_i(k) = \sum_{j=1}^{N} a_{ij}(\chi_k) \times (x_i(k^i_{m_i}) - x_j(k^j_{m_j})) + \theta_i(\chi_k)(x_i(k^i_{m_i}) - x_0(k))$, where $m_j = \arg\min_\epsilon \{k - k^j_\epsilon | k \geq k^j_\epsilon, \epsilon \in N^+\}$. Setting $\phi_i(k) = e_i^T(k)\Omega(\chi_k)e_i(k) - \delta_i(\chi_k)v_i^T(k)\Omega(\chi_k)v_i(k)$ and the next triggered instant $k^i_{m_i+1}$ for clock node i is

$$k^i_{m_i+1} = k^i_{m_i} + \min\{l_i | \phi_i(k^i_{m_i} + l_i) \geq 0, l_i \in N^+\} \tag{9}$$

where, l_i represents the event-triggered time interval.

Remark 1. The above event-triggered scheme decides whether the clock value and clock rate are transmitted to the local controller and its neighboring clock nodes. The condition (8) means the clock value and clock rate of a clock node are not transmitted to its neighboring clock nodes if the clock change is in the allowable range, which can reduce the packet transmission and controller updating. In addition, for the discrete clock systems, one has $k^i_{m_i+1} - k^i_{m_i} \geq h$, which means the Zeno-behavior is not occurred.

Then we define the clock offset $\Delta c_i(k)$ as the difference of the unperfected clock value $c_i(k)$ and the reference clock value $c_0(k)$. It means

$$\Delta c_i(k) = c_i(k) - c_0(k). \tag{10}$$

Similarly, set the clock skew $\Delta\gamma_i(k)$ as the difference of the unperfected clock rate $\gamma_i(k)$ and the reference clock rate $\gamma_0(k)$. It yields

$$\Delta\gamma_i(k) = \gamma_i(k) - \gamma_0(k). \tag{11}$$

The clock synchronization strategy needs to adjust the clock offset and clock skew of each unperfected clock node converged to zero. In addition, the effect of the phase noise $\omega_{ci}(k)$ and the rate noise $\omega_{\gamma i}(k)$ should be reduced. Set $\tilde{x}_i(k) = [\Delta c_i(k), \Delta c_i(k)]^T = x_i(k) - x_0(k)$, the above description can be represented as $\lim_{k\to\infty} \|\tilde{x}_i(k)\| = 0$.

Hence, the objectives of clock synchronization for high-precise clock systems with switching topologies can be given as follows:

(1) For the convergence of clock offset and clock skew, design an event-triggered controller for each unperfected clock node which achieves $\lim_{k\to\infty} \mathbb{E}\|\tilde{x}_i(k)\| = 0$.

(2) To reduce the effect of the phase noise and rate noise, the clock systems should meet the H_∞ performance.

(3) For the optimization of clock offset, clock skew, and control input, investigate a related objective function and optimize the function.

For above objective (3), the objective function is represented as:

$$J = \sum_{k=0}^{\infty} \mathbb{E}\{\sum_{i=1}^{N} \{\tilde{x}_i^T(k) Q \tilde{x}_i(k) + u_i^T(k) R u_i(k)\}\} \tag{12}$$

where, $Q, R \in R^{2\times 2}$ are set as positive matrices.

With switching topologies, the event-triggered controller for clock i is designed as

$$u_i(k) = K(\chi_k) \sum_{j=1}^{N} a_{ij}(\chi_k)[x_i(k^i_{m_i}) - x_j(k^j_{m_j})] + K(\chi_k)\theta_i(\chi_k)[x_i(k^i_{m_i}) - x_0(k)] \tag{13}$$

where, $K(\chi_k)$ is the controller gain for switching topologies. In addition, $a_{ij}(\chi_k)$ and $\theta_i(\chi_k)$ are also varying with different topologies.

With the unperfected clock model (5), clock state change (7), and controller (13), the clock state of clock node i is represented as

$$\begin{aligned} x_i(k+1) =& Ax_i(k) + BK(\chi_k) \sum_{j=1}^{N} a_{ij}(\chi_k)[x_i(k) - x_j(k)] + \\ & BK(\chi_k)\theta_i(\chi_k)[x_i(k) - x_0(k)] - \\ & BK(\chi_k) \sum_{j=1}^{N} a_{ij}(\chi_k)[e_i(k) - e_j(k)] - \\ & BK(\chi_k)\theta_i(\chi_k)e_i(k) + \omega_i(k). \end{aligned} \tag{14}$$

Then, for the description of whole high-precise clock systems with a reference clock node and N unperfected clock nodes, set $\tilde{X}(k) = [\tilde{x}_1^T(k), \tilde{x}_2^T(k), ..., \tilde{x}_N^T(k)]^T$, $\tilde{E}(k) = [e_1^T(k), e_2^T(k), ..., e_N^T(k)]^T$, $\tilde{W}(k) = [\omega_1^T(k), \omega_2^T(k), ..., \omega_N^T(k)]^T$. As a result, the high-precise clock systems can be given as

$$\tilde{X}(k+1) = [I_N \otimes A + H(\chi_k) \otimes BK(\chi_k)]\tilde{X}(k) - H(\chi_k) \otimes BK(\chi_k)\tilde{E}(k) + \tilde{W}(k) \tag{15}$$

where $H(\chi_k) = L(\chi_k) + \Theta(\chi_k)$, $\otimes$ is the Kronecker product, and I_N is the N-dimensional identity matrix.

For the objective function (12), it is converted as

$$\begin{aligned} J = \sum_{k=0}^{\infty} \mathbb{E}\{& \tilde{X}^T(k)(I_N \otimes Q)\tilde{X}(k) + [\tilde{X}(k) - \tilde{E}(k)]^T [H^T(\chi_k)H(\chi_k) \otimes K^T(\chi_k)RK(\chi_k)] \times \\ & [\tilde{X}(k) - \tilde{E}(k)]\}. \end{aligned} \tag{16}$$

Hence, the clock synchronization for high-precise clock systems is transformed as the stability problem of (15). Then, the stability of clock systems (15) and the optimization of (16) will be analyzed.

3. Main results

The sufficient condition for the stable of clock systems (15) is first analyzed in this section. Then, the H_∞ performance for phase noise and rate noise is provided. Afterwards, the optimization problem for obtaining event-triggered weighting matrices and controller gains is solved.

Theorem 1. *With the given parameter matrix $\delta = diag\{\delta_1(\chi_k), \delta_2(\chi_k), ..., \delta_N(\chi_k)\}$ and under the event-triggered condition (8), the clock systems (15) are asymptotically stable when there are no phase noise and rate noise, if there exists $P(\chi_k) > 0$ and the following condition holds*

$$\begin{bmatrix} \Pi_1 - P(\chi_k) + \tilde{S} + \tilde{Q} + \tilde{R} & * \\ \Pi_2 - \tilde{R} - \tilde{S} & \Pi_3 + \tilde{R} + \tilde{S} \end{bmatrix} < 0 \tag{17}$$

where $\Pi_1 = [\tilde{A} + \tilde{H}(\chi_k)]^T P'[\tilde{A} + \tilde{H}(\chi_k)]$, $\Pi_2 = -\tilde{H}^T(\chi_k)P'[\tilde{A} + \tilde{H}(\chi_k)]$, $\Pi_3 = \tilde{H}^T(\chi_k)P'\tilde{H}(\chi_k) - I_N \otimes \Omega(\chi_k)$, $\tilde{A} = I_N \otimes A$, $\tilde{H}(\chi_k) = H(\chi_k) \otimes BK(\chi_k)$, $\tilde{S} = H^T(\chi_k)\delta H(\chi_k) \otimes \Omega(\chi_k)$, $\tilde{Q} = I_N \otimes Q$, $\tilde{R} = H^T(\chi_k)H(\chi_k) \otimes K^T(\chi_k)RK(\chi_k)$, $P' = \sum_{\chi_{k+1}=1}^{q} \pi_{\chi_k\chi_{k+1}} P(\chi_{k+1})$. In addition, $*$ is the symmetric element.

Proof. For the clock systems (15), a stochastic Lyapunov function is designed as

$$V(k) = \tilde{X}^T(k)P(\chi_k)\tilde{X}(k). \tag{18}$$

With the clock systems (15), the difference of (18) is calculated as

$$\begin{aligned} \Delta V(k) =& \mathbb{E}[V(k+1)] - V(k) \\ =& \tilde{X}^T(k+1)\mathbb{E}[P(\chi_{k+1})]\tilde{X}(k+1) - \tilde{X}^T(k)P(\chi_k)\tilde{X}(k) \\ =& \tilde{X}^T(k)\Pi_1\tilde{X}(k) + \tilde{E}^T(k)\tilde{H}^T(\chi_k)P'\tilde{H}(\chi_k)\tilde{E}(k) + \\ & 2\tilde{E}^T(k)\Pi_2\tilde{X}(k) - \tilde{X}^T(k)P(\chi_k)\tilde{X}(k). \end{aligned} \tag{19}$$

For clock node i, when $k_m^i \le k < k_{m+1}^i$ and with inequation (8), one can see that

$$\sum_{i=1}^{N} \phi_i(k) = \sum_{i=1}^{N} [e_i^T(k)\Omega(\chi_k)e_i(k) - \delta_i(\chi_k)v_i^T(k)\Omega(\chi_k)v_i(k)] < 0. \tag{20}$$

For the whole clock systems, it has

$$[\tilde{X}(k) - \tilde{E}(k)]^T \tilde{S}[\tilde{X}(k) - \tilde{E}(k)] - \tilde{E}^T(k)(I_N \otimes \Omega(\chi_k))\tilde{E}(k) > 0. \tag{21}$$

Then with (19) and (21), if (17) is satisfied, we can have

$$\begin{aligned} \Delta V(k) <& \tilde{X}^T(k)\Pi_1\tilde{X}(k) + \tilde{E}^T(k)\Pi_3\tilde{E}(k) + \\ & + 2\tilde{E}^T(k)\Pi_2\tilde{X}(k) + [\tilde{X}(k) - \tilde{E}(k)]^T\tilde{S} \times \\ & [\tilde{X}(k) - \tilde{E}(k)] - \tilde{X}^T(k)P(\chi_k)\tilde{X}(k) \\ <& -\{\tilde{X}^T(k)\tilde{Q}\tilde{X}(k) + [\tilde{X}(k) - \tilde{E}(k)]^T\tilde{R}[\tilde{X}(k) - \tilde{E}(k)]\}. \end{aligned} \tag{22}$$

By defining $\Psi(k) = [\tilde{X}^T(k), \tilde{E}^T(k)]^T$ and with (22), one can obtain

$$\Delta V(k) < \Psi^T(k) \begin{bmatrix} \Pi_1 - P(\chi_k) + \tilde{S} + \tilde{Q} + \tilde{R} & * \\ \Pi_2 - \tilde{R} - \tilde{S} & \Pi_3 + \tilde{R} + \tilde{S} \end{bmatrix} \Psi(k). \tag{23}$$

If (17) in Theorem 1 is satisfied, it means $\Delta V(k) < 0$ and we have

$$\lim_{k\to\infty} \mathbb{E}[V(k)] = 0. \tag{24}$$

Therefore, we achieve

$$\lim_{k\to\infty} \mathbb{E}[\|\tilde{x}_i(k)\|] = 0. \tag{25}$$

With equation (25), the clock offset and clock skew of each unperfected node can converge to zero. Besides, the clock systems (15) are asymptotic stable. The clock synchronization for high-precise clock systems is achieved. Next, considering the nonzero phase noise and rate noise, the analyzation of H_∞ performance for the effect of phase noise and rate noise is given in Theorem 2. □

Theorem 2. *With the given parameter matrix $\delta = diag\{\delta_1(\chi_k), \delta_2(\chi_k), ..., \delta_N(\chi_k)\}$ and under the event-triggered condition (8), the clock systems (15) are stable and meet H_∞ performance with positive parameter η, if there exists $P(\chi_k) > 0$ and the following condition holds*

$$\begin{bmatrix} \Pi_4 & * & * \\ \Pi_2 - \tilde{R} - \tilde{S} & \Pi_3 + \tilde{R} + \tilde{S} & * \\ P'[\tilde{A} + \tilde{H}(\chi_k)] & -P'\tilde{H}(\chi_k) & -\eta^2 I_{2N} + P' \end{bmatrix} < 0 \tag{26}$$

where $\Pi_4 = \Pi_1 - P(\chi_k) + \tilde{S} + \tilde{Q} + \tilde{R} + I_{2N}$.

In addition, the upper bound of (16) is

$$\sup J = \tilde{X}^T(0) P(\chi_0) \tilde{X}(0). \tag{27}$$

Proof. Set $\Phi(k) = [\Psi^T(k), \tilde{W}^T(k)]^T$. For the nonzero phase noise and rate noise under zero-initial condition, we can conclude that

$$\Delta V(k) + \tilde{X}^T(k)\tilde{X}(k) - \eta^2 \tilde{W}^T(k)\tilde{W}(k) < \Phi^T(k) \begin{bmatrix} \Pi_4 & * & * \\ \Pi_2 - \tilde{R} - \tilde{S} & \Pi_3 + \tilde{R} + \tilde{S} & * \\ P'[\tilde{A} + \tilde{H}(\chi_k)] & -P'\tilde{H}(\chi_k) & -\eta^2 I_{2N} + P' \end{bmatrix} \Phi(k). \tag{28}$$

If (26) in Theorem 2 is satisfied, it has

$$\Delta V(k) + \tilde{X}^T(k)\tilde{X}(k) - \eta^2 \tilde{W}^T(k)\tilde{W}(k) < 0. \tag{29}$$

For k from zero to infinite, we have

$$\sum_{k=0}^{\infty} \{\Delta V(k) + \tilde{X}^T(k)\tilde{X}(k) - \eta^2 \tilde{W}^T(k)\tilde{W}(k)\} < 0. \tag{30}$$

With zero-initial condition, one has

$$\sum_{k=0}^{\infty} \sum_{i=1}^{N} [\tilde{x}_i^T(k)\tilde{x}_i(k) - \eta^2 \omega_i^T(k)\omega_i(k)] < 0. \tag{31}$$

Hence, the clock systems (15) meet H_∞ performance, which means the effect of the phase noise and rate noise can be reduced. Then on the basis of defined condition

$$\Delta V(k) < -\{\tilde{X}^T(k)\tilde{Q}\tilde{X}(k) + [\tilde{X}(k) - \tilde{E}(k)]^T \tilde{R}[\tilde{X}(k) - \tilde{E}(k)]\}, \tag{32}$$

and by accumulating (32) from zero to infinite, one has

$$J = \mathbb{E}[V(0)] = \mathbb{E}[\tilde{X}^T(0) P(\chi_0) \tilde{X}(0)]. \tag{33}$$

Therefore, the upper bound of objective function can be achieved as (27).

For obtaining event-triggered weighting matrices and controller gains, we give Theorem 3 to solve the nonlinear terms of (26) in Theorem 2. □

Theorem 3. *With the given parameter matrix $\delta = diag\{\delta_1(\chi_k), \delta_2(\chi_k), ..., \delta_N(\chi_k)\}$ and under the event-triggered condition (8), the event-triggered weighting matrices and controller gains are solvable, if there exist $P(\chi_k) > 0$, $Y(\chi_k) > 0$ and the following condition holds*

$$\begin{bmatrix} \Pi_5 & * & * & * & * \\ -\tilde{S} & -I_N \otimes \Omega(\chi_k) + \tilde{S} & * & * & * \\ 0 & 0 & -\eta^2 I_{2N} & * & * \\ \tilde{K}(\chi_k) & -\tilde{K}(\chi_k) & 0 & -\bar{R}^{-1} & * \\ \pi_{\chi_k} \otimes \Pi_6 & -\pi_{\chi_k} \otimes \Pi_7 & \pi_{\chi_k} \otimes I_{2N} & 0 & -\tilde{Y} \end{bmatrix} < 0 \tag{34}$$

where $\Pi_5 = -P(\chi_k) + \tilde{S} + \tilde{Q} + I_{2N}$, $\Pi_6 = \tilde{A} + \bar{H}(\chi_k)\bar{K}(\chi_k)$, $\Pi_7 = \bar{H}(\chi_k)\bar{K}(\chi_k)$, $\bar{H}(\chi_k) = H(\chi_k) \otimes B$, $\bar{K}(\chi_k) = I_N \otimes K(\chi_k)$, $\pi_{\chi_k} = [\pi_{\chi_k 1}^{0.5}, \pi_{\chi_k 2}^{0.5}, ..., \pi_{\chi_k q}^{0.5}]^T$, $\tilde{Y} = diag\{Y(1), Y(2), ..., Y(q)\}$, $Y(\chi_k) = P^{-1}(\chi_k)$, *and* $\bar{R} = H^T(\chi_k)H(\chi_k) \otimes R$.

Proof. The inequation (26) is converted as

$$\begin{bmatrix} \Pi_5 & * & * \\ -\tilde{S} & -I_N \otimes \Omega(\chi_k) + \tilde{S} & * \\ 0 & 0 & -\eta^2 I_{2N} \end{bmatrix} + \Pi_8^T \bar{R} \Pi_8 + \Pi_9^T P' \Pi_9 < 0, \tag{35}$$

where, $\Pi_8 = [\bar{K}(\chi_k), -\bar{K}(\chi_k), 0]$, $\Pi_9 = [A + \bar{H}(\chi_k)\bar{K}(\chi_k), -\bar{H}(\chi_k)\bar{K}(\chi_k), I_{2N}]$

Through inequation (35) and utilizing the Schur complement [31], the Theorem 3 can be obtained.

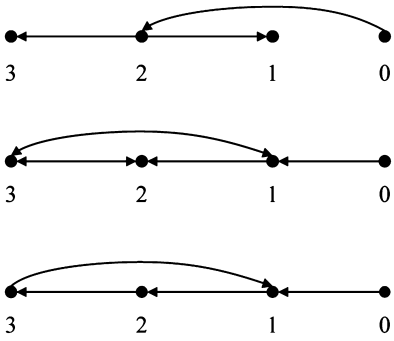

Fig. 1. Possible topologies of clock systems.

Then we optimize the objective function. First, set $\tilde{X}^T(0)P(\chi_0)\tilde{X}(0) \leq \Gamma$, the minimization of (27) can be converted into

$$\begin{aligned} &\min \ \ \Gamma \\ &\text{s.t.} \ \ \tilde{X}^T(0)P(\chi_0)\tilde{X}(0) \leq \Gamma. \end{aligned} \tag{36}$$

The constraint condition in optimization problem (36) can be represented as

$$\begin{bmatrix} \Gamma & * \\ \tilde{X}(0) & Y(\chi_k) \end{bmatrix} \geq 0. \tag{37}$$

For the constraints $Y(\chi_k) = P^{-1}(\chi_k)$, it can be converted as the rank constrained linear matrix inequalities as follows [32]

$$\begin{bmatrix} P(\chi_k) & * \\ I & Y(\chi_k) \end{bmatrix} \geq 0, rank \begin{bmatrix} P(\chi_k) & * \\ I & Y(\chi_k) \end{bmatrix} \leq 2N. \tag{38}$$

As a result, the clock synchronization strategy for clock systems in WSN can be described as the follow optimization problem (39).

$$\begin{aligned} &\min \ \ \Gamma \\ &\text{s.t.} \ \ (15),\ (34),\ (37),\ \text{and}\ (38). \ \square \end{aligned} \tag{39}$$

Remark 2. By solving the optimization problem (39), the event-triggered weighting matrices and controller gains can be obtained as well as the optimization of the objective function. In addition, the solution of (39) can achieve the convergence of clock offset and clock skew, and reduce the effect of phase noise and rate noise. It means all control objectives are achieved.

4. Numerical example

In this section, we conduct numerical experiments to validate the proposed event-triggered clock synchronization strategy for high-precise clock systems. In the example, we give the clock systems which contains four clock nodes with a reference node and three unperfected clock nodes.

We set that the communication topologies of clock systems switch from three possible topologies which are shown in Fig. 1 and define as $\tilde{G}(1)$, $\tilde{G}(2)$, $\tilde{G}(3)$. With Fig. 1, the clock 0 is the reference clock node, and others are unperfected nodes which need to be synchronized.

The switching topologies are driven by a Markov chain and the transition probability matrix is $\pi = \begin{bmatrix} 0.5 & 0.3 & 0.2 \\ 0.3 & 0.6 & 0.1 \\ 0.3 & 0.3 & 0.4 \end{bmatrix}$. In addition, $\tilde{G}(1)$ is the initial topology.

For the entire clock systems, the initial clock offsets and skew values of nodes 1, 2, and 3 are given in Table 1. The phase noise $\omega_{ci}(k)$ and the clock rate noise $\omega_{\gamma i}(k)$ are assumed as Gussian noise with zero mean value and the standard deviation is 10^{-6}. The event-triggered parameters are designed as $\delta_i(1) = 0.055$, $\delta_i(2) = 0.045$, and $\delta_i(3) = 0.095$, $(i = 1, 2, 3)$ for $\tilde{G}(1)$, $\tilde{G}(2)$, $\tilde{G}(3)$, respectively. The weighting matrices of (12) is set as $Q = 10I_2$ and $R = 2I_2$.

The simulation time is set as 30 seconds. In Fig. 2, topologies $\tilde{G}(1)$, $\tilde{G}(2)$, and $\tilde{G}(3)$ are shown as modes 1, 2 and 3, respectively. It can be seen the Markov switching sequences clearly. By solving the optimization problem (39), we can obtain the controller gains $K(1) = \begin{bmatrix} -0.0579 & -0.0058 \\ 0 & -0.058 \end{bmatrix}$, $K(2) = \begin{bmatrix} -0.0816 & -0.008 \\ 0.0001 & -0.0817 \end{bmatrix}$, and $K(3) = \begin{bmatrix} -0.0866 & -0.0085 \\ 0.002 & -0.0868 \end{bmatrix}$. In addition, the event-triggered weighting matrices $\Omega(1) = \begin{bmatrix} 9.1092 & 0.4916 \\ 0.4916 & 9.4418 \end{bmatrix}$, $\Omega(2) = \begin{bmatrix} 14.1649 & 0.7462 \\ 0.7462 & 14.6778 \end{bmatrix}$, and $\Omega(3) = \begin{bmatrix} 10.2542 & 0.5325 \\ 0.5325 & 10.6245 \end{bmatrix}$.

Table 1
Initial clock offset and skew values.

node	value
Offset of node 1	8.3s
Offset of node 2	5.2s
Offset of node 3	6.6s
Skew of node 1	0.1
Skew of node 2	0.2
Skew of node 3	0.15

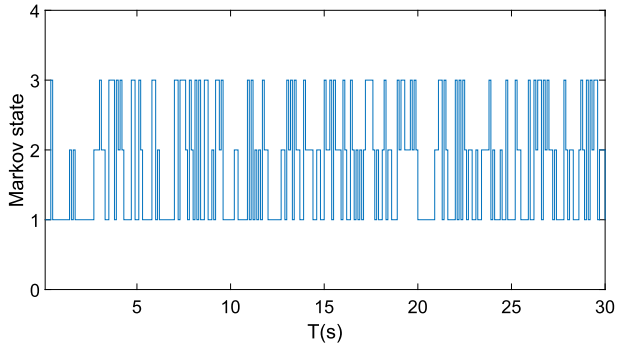

Fig. 2. Markov switching sequences.

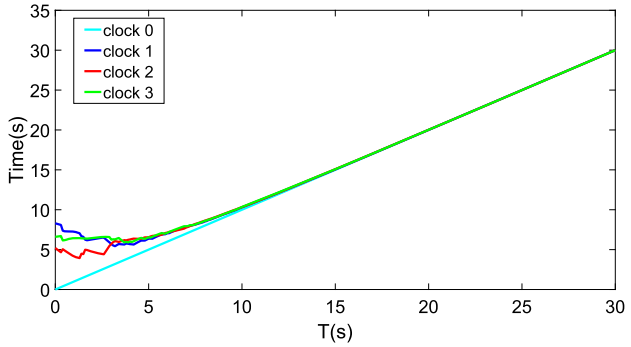

Fig. 3. Clock times of clock systems.

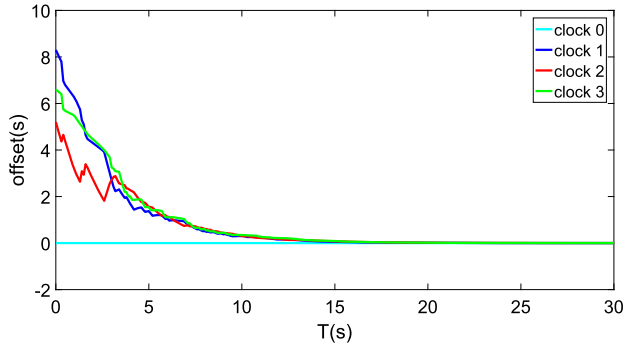

Fig. 4. Offsets of clock systems.

In the example, the clock times of clock systems are shown in Fig. 3. From Fig. 3, one can see that the clock times of unperfected clock nodes can be synchronized with the reference clock. The Fig. 4 and Fig. 5 give the offsets and skews of clock systems. The offsets and skews of unperfected clock nodes can be converged. In Fig. 6, a small segment of the clock offsets at the steady synchronization state is intercepted. From Fig. 6, we can find that the synchronization accuracy reaches microsecond level. It means the proposed method in this paper can achieve clock synchronization for high-precise clock systems.

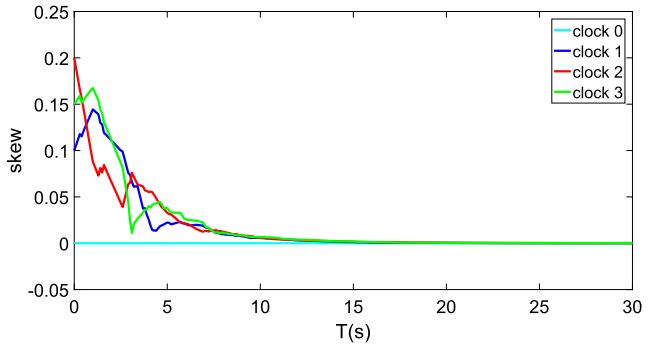

Fig. 5. Skews of clock systems.

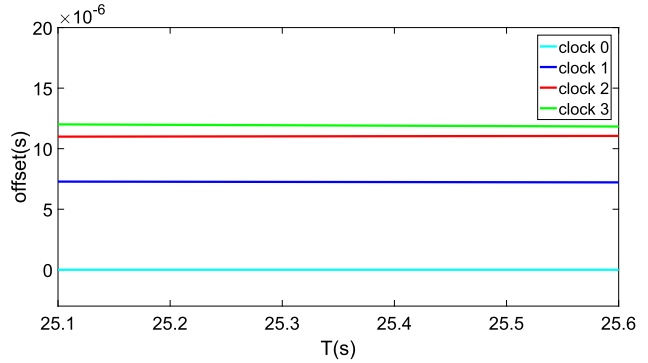

Fig. 6. Clock offsets at the steady synchronization state.

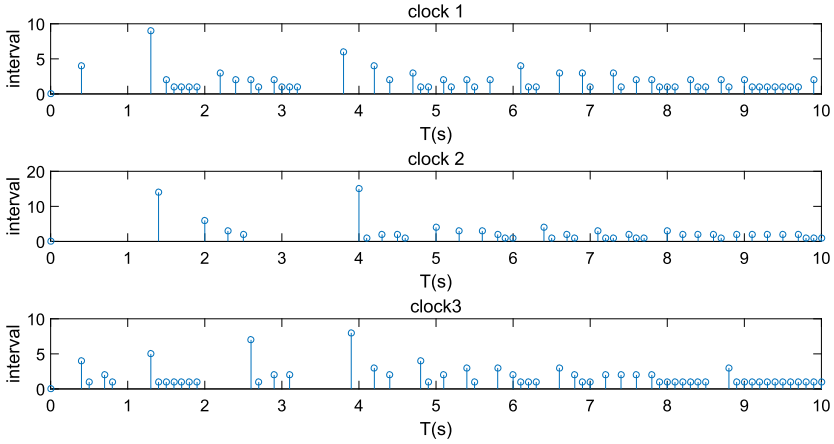

Fig. 7. Transmission instants and intervals of unperfected clocks.

The triggered instants and intervals of unperfected clocks are shown in Fig. 7. In Fig. 7, we give the triggered instants and intervals for first 10 seconds. With the unperfected clock nodes, the number of triggered instants is 38, 31, and 49 for unperfected clock nodes 1, 2, and 3, respectively. Comparing with the number of samples, the number of transmitted data is significantly reduced for each unperfected clock node.

Then, the comparation results with sample-data strategy are shown in Fig. 8 and Fig. 9. The Fig. 8 and Fig. 9 show the offsets and skews of clock nodes under the sample-data strategy. For the proposed clock synchronization strategy and the sample-data strategy, the only difference is the sample-data strategy needs all sampling information. With Fig. 4, Fig. 5, Fig. 8, and Fig. 9, both two strategies can achieve clock synchronization. The proposed clock synchronization strategy can have the almost same performance with less clock data.

Afterwards, we give a comparation with the method in reference [27]. With the same initial condition, the simulation results of reference [27] are shown in Figs. 10 and 11. Although the results in reference [27] can achieve the clock synchronization, the

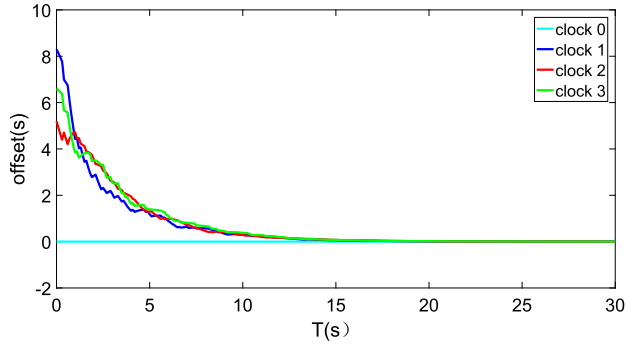

Fig. 8. Offsets of clock systems with sample-data strategy.

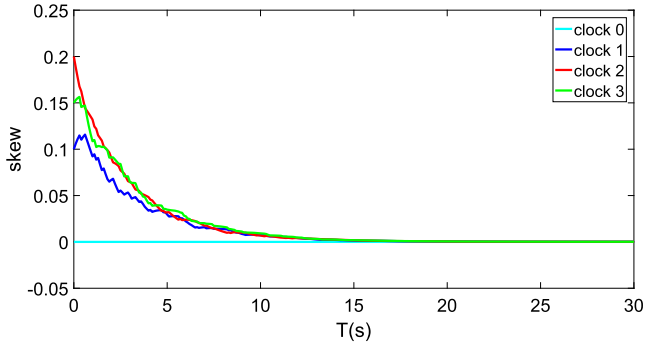

Fig. 9. Skews of clock systems with sample-data strategy.

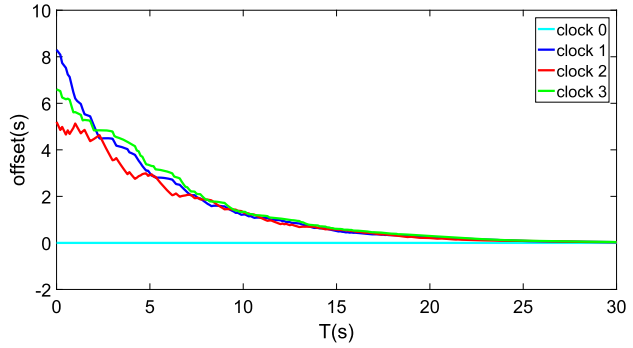

Fig. 10. Offsets of clock systems with reference [27].

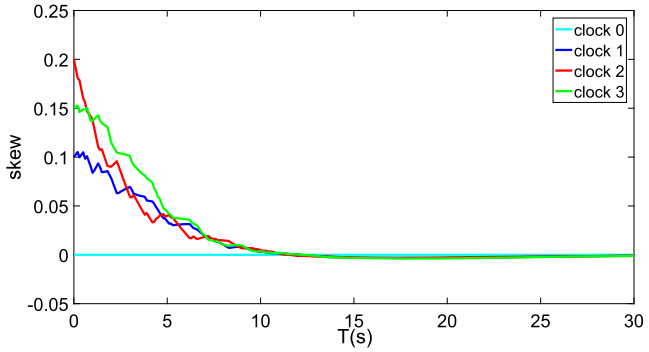

Fig. 11. Skews of clock systems with reference [27].

synchronization speed is slower than the proposed clock synchronization strategy. Obviously, the proposed strategy is more suitable for clock synchronization of high-precise clock systems with switching topologies.

5. Conclusion

In this paper, an accurate event-triggered clock synchronization mechanism for high-precise clock systems with switching topologies is presented. The event-triggered synchronization method can make the communication and computation more efficient, and reduce the number of packet exchanges. According to the proposed clock synchronization scheme, the offsets and skews of clocks systems can converge to zero which means the high-precise clock synchronization can be achieved. In addition, the effect of phase noise and rate noise can be reduced. However, the communication delay in high-precise clock systems is an essential factor which need to be fully considered and it is different from the general multi-agent systems. In the future work, we will consider the communication delay of the high-precise clock systems.

CRediT authorship contribution statement

Hui Zhao: Writing – review & editing, Writing – original draft, Software, Methodology. **Xuewu Dai:** Writing – review & editing, Conceptualization. **Yuan Zhao:** Writing – review & editing, Writing – original draft.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability statement

The authors confirm that the data supporting the findings of this study are available within the article.

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